MODULE A · OCR J277 1.1 · CAMBRIDGE 0478 3.1

Systems architecture

The **CPU**, its **registers**, **Von Neumann** architecture, the **fetch-execute cycle**, **performance** and **embedded systems**. Spec versions as checked in November 2026.

01 Computer system and CPU (A1)

Computer system Hardware and software working together: input, process, output or store.

Hardware / software Physical parts / programs (sets of instructions).

CPU Processes instructions and data that are input so the result can be output.

Purpose Runs programs by fetching and executing instructions held in RAM.

02 Inside the CPU (A2)

ALU Arithmetic, logic and comparisons.

Control unit Decodes instructions; sends control signals.

Cache Small fast memory for frequently used data/instructions (OCR lists it as a CPU component; Cambridge covers it under performance).

PC Address of the next instruction.

MAR Address being read from or written to.

MDR Data or instruction fetched from / to be written to memory.

Accumulator Results of ALU operations.

CIR IGCSE only Instruction being decoded and executed.

03 Fetch-execute cycle (A4) · OCR "fetch-execute", Cambridge "fetch-decode-execute"

01

Fetch

Instruction fetched from RAM using the address in the PC; PC incremented. **IGCSE:** PC → MAR → address bus; data bus → MDR → CIR.

02

Decode

The CU works out what the instruction means. **IGCSE:** decodes the CIR.

03

Execute

ALU calculates or data is loaded/stored; ALU results in the accumulator. Then repeat. OCR does not need register-to-register transfers.

04 Von Neumann and buses (A3)

Von Neumann Instructions and data stored together in the same main memory.

Stored program Program loaded into memory; instructions fetched and executed in turn.

Address vs data Address = where; data = the value stored there.

Address bus IGCSE only MAR to memory. One-way.

Data bus IGCSE only Data/instructions between memory and MDR. Two-way.

Control bus IGCSE only Control signals (read, write, clock). Two-way.

05 CPU performance (A5)

Clock speed Cycles per second (Hz). 3.5 GHz = 3.5 billion/s. Higher = more instructions per second.

Number of cores More instructions at the same time, if software can split the task.

Cache size More data found in cache, fewer slower fetches from RAM.

Combined GCSE only Compare changes on their own and together, e.g. 4 cores at 2 GHz vs 2 at 3.5 GHz.

Units OCR: 1 KB = 1,000 bytes. Cambridge: 1 KiB = 1,024 bytes.

06 Embedded systems (A6)

- **Embedded**

  Dedicated function inside a larger device. Small, low power, low cost, reliable, often real-time; program in ROM. E.g. washing machine, thermostat.

- **General purpose**

  Runs many different programs. E.g. laptop, desktop PC.

07 Instruction sets (A7) IGCSE only

Microprocessor Integrated circuit on a single chip that acts as the CPU.

Instruction set All the commands a CPU can process; machine code (binary).

Why it matters A CPU only runs instructions from its own set.

01

The CPU fetches **instructions and data**, never "programs" or "information".

02

The PC holds the **address of the next instruction**; it does not count programs.

03

Say **clock speed**, **number of cores**, **cache size**, not just "clock", "cores", "cache".

04

Embedded = **dedicated function within a larger device**, applied to the device in the question.