CAMBRIDGE IGCSE (0478)

Module A: Systems architecture

Workbooklet mark scheme · 7 parts · 140 marks

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	Total	**140**

MODULE A SYSTEMS ARCHITECTURE · A1

What a computer system is and what the CPU does: mark scheme

~25 minutes · 20 marks · Cambridge 0478 syllabus 3.1.1(a)

How to use. Mark positively. "Any N from" means award one mark per point up to N. **//** separates alternative answers for the same mark. Words in (brackets) are not needed for the mark. Credit any other valid answer that shows the same understanding.

QUESTION	ANSWER	MARKS	GUIDANCE
1(a) 0478 3.1.1(a)	Central processing unit	**1**	All three words needed.
1(b) 0478 3.1.1(a)	Any **two** from: It processes instructions and data // it runs the kiosk's program ... that are input (e.g. the scanned ticket code) ... so that the result can be output (e.g. the map shown on the screen / the description played) It fetches, decodes and executes instructions	**2**	max 2. Do not accept "it stores the map images" or "it controls the computer" alone.
1(c) 0478 3.1.1(a)	Barcode scanner: Input Screen: Output Speaker: Output Hard disk drive: Storage	**4**	1 mark per correct row. More than one tick in a row: no mark for that row.
2(a) 0478 3.1.1(a)	Fetch-decode-execute cycle	**1**	More than one tick: 0.
2(b) 0478 3.1.1(a)	RAM // random access memory fetches decodes executes	**4**	1 mark per correct word. Accept "gets / retrieves" for fetches; "interprets" for decodes; "runs / carries out" for executes. Do not accept "ROM" or "storage" for the first blank.
3 0478 3.1.1(a)	Any **three** from: Fetch: an instruction is fetched from (main) memory / RAM Decode: the instruction is decoded // the CPU works out what the instruction means (by the control unit) Execute: the instruction is carried out The cycle repeats (for the next instruction)	**3**	max 3. Naming the three stages only, with no description, scores 1. Credit correct register/bus detail (taught in A3/A4) but it is not needed.

QUESTION	ANSWER	MARKS	GUIDANCE
4 0478 3.1.1(a)	Any **three** from: The scanner inputs the image (as data) The CPU processes the data (that has been input) ... by running / executing the instructions of the (scanning) program ... (fetching, decoding and executing them) ... so that the result / processed image can be output (to the monitor) Without the CPU the input data could not be processed // nothing would be output	**3**	max 3. Answer must be linked to the scenario for full marks. Do not accept "the CPU stores the invoice".
5 0478 3.1.1(a)	The CPU processes instructions and data. The CPU repeats the FDE cycle for each instruction in a program.	**2**	1 mark per correct tick. More than two ticks: 0.

Total: 20 marks

MODULE A SYSTEMS ARCHITECTURE · A2

Inside the CPU: mark scheme

~25 minutes · 20 marks · Cambridge syllabus 3.1.2(a), 3.1.3

How to use. Award one mark per creditworthy point up to the maximum shown. **/** separates alternative words; **//** separates alternative answers for the same point. Words in (brackets) are not needed for the mark.

QUESTION	ANSWER	MARKS	GUIDANCE
1(a) 0478 3.1.2(a)	Arithmetic logic unit // ALU	**1**	
1(b) 0478 3.1.2(a)	Any two from: Arithmetic // calculations, e.g. subtracting arrival time from leaving time // working out the charge Logic // comparisons, e.g. checking whether the stay is longer than a time limit // whether the amount paid is enough Logical operations // AND / OR / NOT	**2**	max 2
2(a) 0478 3.1.2(a)	One mark for each correct row: PC: Address MAR: Address MDR: Data CIR: Data ACC: Data	**5**	Two ticks in a row: no mark for that row.
3(a) 0478 3.1.2(a)	One mark for each correct register: Program counter // PC Current instruction register // CIR Accumulator // ACC Memory address register // MAR	**4**	
4(a) 0478 3.1.2(a)	Any three from: Decodes instructions // works out what each instruction means Sends control signals (to other components) Controls / coordinates the other components // the ALU, registers and memory Controls the flow of data (within the CPU / between the CPU and memory) Manages the fetch–decode–execute cycle	**3**	max 3
5(a) 0478 3.1.2(a)	In the MAR, 40 is an address // the location in memory to be read from / written to In the MDR, 40 is data / an instruction // the value read from / to be written to (that) memory location	**2**	

QUESTION	ANSWER	MARKS	GUIDANCE
6(a) 0478 3.1.3	Any three from: Cache is (small, fast) memory in / close to the CPU It stores frequently used data / instructions Cache is faster to access than RAM ... so the CPU does not need to fetch them from (slower) RAM // fewer RAM accesses Larger cache can store more frequently used data / instructions	**3**	max 3

Total: 20 marks

MODULE A SYSTEMS ARCHITECTURE · A3

Von Neumann architecture and the buses: mark scheme

~25 minutes · 20 marks · 0478 syllabus 3.1.2(a)

How to use. Award one mark per creditworthy point up to the maximum shown. **/** separates alternative words; **//** separates alternative answers for the same point. Words in (brackets) are not needed for the mark. "..." means the point builds on the one before. Credit any other valid answer that shows the same understanding.

QUESTION	ANSWER	MARKS	GUIDANCE
1(a) 0478 3.1.2(a)	Any one from: Instructions and data are stored in the same memory / RAM Programs are stored in memory (stored program concept) Instructions and data are fetched from the same memory // share the same buses	**1**	max 1
1(b) 0478 3.1.2(a)	Program counter / PC Memory address register / MAR	**2**	One mark each. First two answers only.
2(a) 0478 3.1.2(a)	Memory data register / MDR Current instruction register / CIR Program counter / PC Accumulator / ACC	**4**	One mark for each correct row, in order.
3(a) 0478 3.1.2(a)	Read or write signal: control bus Location MAR points to: address bus Instruction from RAM to MDR: data bus One direction only: address bus Value from MDR to RAM: data bus	**5**	One mark for each correct row. More than one tick in a row: no mark for that row.
4(a) 0478 3.1.2(a)	Memory address register / MAR	**1**	
4(b) 0478 3.1.2(a)	Any four from: The address (0110 1100) is placed in the MAR The address is sent (from the MAR) to RAM along the address bus The control unit sends a read signal along the control bus The price / data stored at that address is sent along the data bus ... (from RAM) to the CPU / into the MDR	**4**	max 4. Buses must be named correctly for each point.

QUESTION	ANSWER	MARKS	GUIDANCE
5(a) 0478 3.1.2(a)	Any three from: Data / instructions are read from RAM into the CPU // RAM to MDR Data is also written from the CPU to RAM // MDR to RAM ... so the data bus is bidirectional / two-way Addresses are only sent from the CPU (MAR) to RAM ... RAM never needs to send an address back to the CPU // so the address bus is unidirectional / one-way	**3**	max 3. Must give at least one reason for each bus for full marks.

Total: 20 marks

MODULE A SYSTEMS ARCHITECTURE · A4

The fetch-decode-execute (FDE) cycle: mark scheme

20 marks · Cambridge 0478 syllabus 3.1.2(b)

How to use. One mark per creditworthy point up to the maximum shown. **//** separates alternative answers. Words in (brackets) are not needed for the mark. Credit any other valid answer that shows the same understanding.

QUESTION	ANSWER	MARKS	GUIDANCE
1(a) 0478 3.1.2(b)	Current instruction register // CIR	**1**	Do not accept MDR.
1(b) 0478 3.1.2(b)	Address bus	**1**	More than one tick = 0.
2(a) 0478 3.1.2(b)	program counter // PC MAR address bus data bus MDR CIR	**6**	One mark for each correct term, in this order.
3(a) 0478 3.1.2(b)	PC: address MAR: address CIR: data / instruction ACC: data / instruction	**4**	One mark per correct row. Two ticks in a row = 0 for that row.
4(a) 0478 3.1.2(b)	151	**1**	Correct answer only.
4(b) 0478 3.1.2(b)	Any four from: The CU decodes the instruction (in the CIR) // the CU sends signals to carry it out The address 300 is placed in the MAR 300 is sent along the address bus (to RAM) A read signal is sent along the control bus The value (stored) at address 300 is sent along the data bus The value is stored in the MDR The value is copied from the MDR into the accumulator // ACC	**4**	max 4. Do not award points about fetching the instruction from address 150. Do not accept "300 is loaded into the accumulator" (300 is the address, not the value).

QUESTION	ANSWER	MARKS	GUIDANCE

5(a)
0478 3.1.2(b)
	Any three from:
	Decodes the instruction (held in the CIR) // works out what the instruction means
	Sends control signals (along the control bus) // e.g. read // write signals to memory
	Controls // coordinates the flow of data (and instructions) between the CPU components and memory
	Tells the ALU which operation to carry out
	Makes sure the stages happen in the correct order // in time with the clock
		3	max 3. Do not accept "carries out calculations" (ALU).

Total: 20 marks

MODULE A SYSTEMS ARCHITECTURE · A5

CPU performance: mark scheme

~25 minutes · 20 marks · 0478 syllabus 3.1.3

How to use. Award one mark per creditworthy point up to the maximum shown. **//** separates alternative answers for the same mark. Words in (brackets) are not needed for the mark. Mark positively and credit any other valid answer.

QUESTION	ANSWER	MARKS	GUIDANCE
1(a) 0478 3.1.3	Second row ticked: the number of fetch-decode-execute cycles carried out per second	**1**	More than one tick = 0.
1(b) 0478 3.1.3	2.5 billion // 2 500 000 000 // 2500 million	**1**	
1(c) 0478 3.1.3	Any two from: More (FDE) cycles can be carried out per second So more instructions can be processed/executed per second So tasks/programs are completed in less time	**2**	max 2
2(a) 0478 3.1.3	Any two from: Small (capacity) memory Very fast (to access) // faster than RAM Inside / close to the CPU Stores frequently used data // frequently used instructions	**2**	max 2
2(b) 0478 3.1.3	Any three from: More frequently used data/instructions can be stored in cache Cache is faster to access than RAM So fewer (slower) fetches from RAM are needed // data/instructions are more likely to be found in cache So the CPU spends less time waiting (for data/instructions) So more instructions can be processed in the same time	**3**	max 3
3(a) 0478 3.1.3	Any two from: Each core can fetch, decode and execute instructions (independently) More instructions can be processed at the same time // simultaneously Tasks can be shared / split between the cores	**2**	max 2

QUESTION	ANSWER	MARKS	GUIDANCE
3(b) 0478 3.1.3	Any two from: The program (software) cannot split its task between cores // only uses one core So the extra cores are not used / are idle The clock speed (and cache size) of each core has not changed, so the one core used runs at the same speed	**2**	max 2
4(a) 0478 3.1.3	Row 1: True Row 2: False Row 3: False Row 4: True	**4**	One mark per row. Two ticks in a row = 0 for that row.
5(a) 0478 3.1.3	Cache size // increase the (size of the) cache Any two from: More frequently used data/instructions can be held in cache So fewer fetches from (slower) RAM are needed Cache is faster to access than RAM so the CPU waits less	**3**	1 mark for cache size, then max 2 for the explanation. Clock speed or cores identified = 0 for the whole part.

Total: 20 marks

MODULE A SYSTEMS ARCHITECTURE · A6

Embedded systems: mark scheme

20 marks · Cambridge 0478 syllabus 3.1.5

How to use. One mark per creditworthy point up to the maximum shown. **/** separates alternative words; **//** separates alternative answers. Words in (brackets) are not needed for the mark. Credit any other valid answer that shows the same understanding.

QUESTION	ANSWER	MARKS	GUIDANCE
1(a) 0478 3.1.5	Any two from: To perform a dedicated function // one specific task It is (built) within a larger device / system To control / monitor the device it is part of It is a computer system / has a microprocessor / CPU	**2**	max 2.
2(a) 0478 3.1.5	electric oven street-lighting controller train-ticket machine	**3**	One mark for each correct circle. If more than three are circled, deduct one mark for each extra (minimum 0).
3(a) 0478 3.1.5	Any one from: To open and close the (roof) vents // to control the temperature in the greenhouse // to stop the greenhouse getting too warm	**1**	Must be in context.
3(b) 0478 3.1.5	Any two from: It is a computer system / has a microprocessor It is part of a larger device // built into the vent motor It performs one dedicated function // only opens/closes the vents It cannot be used for other tasks // user cannot install other programs	**2**	max 2.
3(c) 0478 3.1.5	Any two from: Performs a dedicated function / single task Part of a larger device Small (in size) Low power (consumption) Low cost Simple / limited / no user interface Program stored in ROM // firmware // not usually changed by the user Reliable // works in real time	**2**	max 2. Do not award the same idea twice (e.g. "dedicated function" and "single task").

QUESTION	ANSWER	MARKS	GUIDANCE
4(a) 0478 3.1.5	One dedicated function: embedded system Install many applications: general purpose computer Contains a processor: both Built into a larger device: embedded system	**4**	One mark per correct row. More than one tick in a row: 0 for that row.
5(a) 0478 3.1.5	Any four from: The security system's control unit is an embedded system It performs a dedicated function // only monitors the sensors / keypad and sounds the alarm It is part of a larger system // built into the security system Its program is not usually changed by the user // stored in ROM / firmware The PC is a general purpose computer The PC performs many different functions // e.g. drawing plans, email, web browsing The user can install / run different software on the PC	**4**	max 4. max 3 if only the control unit or only the PC is described.
6(a) 0478 3.1.5	Any two from: Engine management // engine control Anti-lock braking (ABS) Airbag control Satnav / GPS Climate control / air conditioning Central locking // alarm // immobiliser Parking sensors Entertainment system / radio // dashboard display	**2**	max 2. Accept any other valid control system in a car. Do not accept a passenger's phone or laptop.

Total: 20 marks

MODULE A SYSTEMS ARCHITECTURE · A7 (IGCSE ONLY)

Instruction sets and microprocessors: mark scheme

20 marks · Cambridge 0478 syllabus 3.1.1(b), 3.1.4

How to use. One mark per creditworthy point up to the maximum shown. **/** separates alternative words; **//** separates alternative answers. Words in (brackets) are not needed for the mark. Credit any other valid answer that shows the same understanding.

QUESTION	ANSWER	MARKS	GUIDANCE
1(a) 0478 3.1.1(b)	Any one from: A (type of) integrated circuit on a single chip // a CPU on a single chip	**1**	Must mention single / one chip. "A small processor" alone is too vague.
1(b) 0478 3.1.4	Any two from: A list of all the commands / instructions ... ... that can be processed by a CPU The commands are (in) machine code / binary	**2**	max 2. "A set of instructions" alone is too vague (0 marks).
2(a) 0478 3.1.1(b), 3.1.4	Integrated circuit on a single chip: True Execute a command not in its set: False Every CPU has the same set: False	**3**	One mark per correct row. Both boxes ticked in a row: 0 for that row.
3(a) 0478 3.1.4	Machine code	**1**	Do not accept "binary" alone (given in the question).
3(b) 0478 3.1.4	Any two from: SUBTRACT is not in the CPU's instruction set A CPU can only process / execute commands in its own instruction set The CPU would not be able to decode it // would not recognise the (machine) code	**2**	max 2.
3(c) 0478 3.1.4	Any three from: LOAD 0 // LOAD 5 (as the starting value) Use ADD repeatedly // repeated addition ... ADD 5 three times (after LOAD 0) // ADD 5 twice (after LOAD 5) // ADD 3 five times (after LOAD 0) OUTPUT the accumulator / result (15)	**3**	max 3. Accept codes (00, 01, 11) in place of command names. Accept STORE used along the way. No mark for any step that uses a command not in the table.
4(a) 0478 3.1.4 (with 3.1.2(b))	One mark for each correct word, in order: RAM decoded control unit executed	**4**	Accept CU for control unit.

QUESTION	ANSWER	MARKS	GUIDANCE
5(a) 0478 3.1.4	Any two from: Load Store Add Subtract Compare Jump // branch Input // output	**2**	max 2. Accept any other valid CPU operation, e.g. AND / OR / shift. Accept a description, e.g. "add two numbers".
6(a) 0478 3.1.4	Any two from: Different types of CPU can have different instruction sets The machine code was written for the desktop CPU's instruction set The phone's CPU can only execute commands from its own instruction set // may not recognise / decode the desktop CPU's commands	**2**	max 2. Do not credit answers about screen size or storage space alone.

Total: 20 marks