MODULE A SYSTEMS ARCHITECTURE · A2

Inside the CPU: mark scheme

~25 minutes · 20 marks · Cambridge syllabus 3.1.2(a), 3.1.3

How to use. Award one mark per creditworthy point up to the maximum shown. **/** separates alternative words; **//** separates alternative answers for the same point. Words in (brackets) are not needed for the mark.

QUESTION	ANSWER	MARKS	GUIDANCE
1(a) 0478 3.1.2(a)	Arithmetic logic unit // ALU	**1**	
1(b) 0478 3.1.2(a)	Any two from: Arithmetic // calculations, e.g. subtracting arrival time from leaving time // working out the charge Logic // comparisons, e.g. checking whether the stay is longer than a time limit // whether the amount paid is enough Logical operations // AND / OR / NOT	**2**	max 2
2(a) 0478 3.1.2(a)	One mark for each correct row: PC: Address MAR: Address MDR: Data CIR: Data ACC: Data	**5**	Two ticks in a row: no mark for that row.
3(a) 0478 3.1.2(a)	One mark for each correct register: Program counter // PC Current instruction register // CIR Accumulator // ACC Memory address register // MAR	**4**	
4(a) 0478 3.1.2(a)	Any three from: Decodes instructions // works out what each instruction means Sends control signals (to other components) Controls / coordinates the other components // the ALU, registers and memory Controls the flow of data (within the CPU / between the CPU and memory) Manages the fetch–decode–execute cycle	**3**	max 3
5(a) 0478 3.1.2(a)	In the MAR, 40 is an address // the location in memory to be read from / written to In the MDR, 40 is data / an instruction // the value read from / to be written to (that) memory location	**2**	

QUESTION	ANSWER	MARKS	GUIDANCE
6(a) 0478 3.1.3	Any three from: Cache is (small, fast) memory in / close to the CPU It stores frequently used data / instructions Cache is faster to access than RAM ... so the CPU does not need to fetch them from (slower) RAM // fewer RAM accesses Larger cache can store more frequently used data / instructions	**3**	max 3

Total: 20 marks