MODULE A SYSTEMS ARCHITECTURE · A2

Inside the CPU: ALU, CU, cache and registers

Original practice questions · ~25 minutes · 20 marks · Cambridge syllabus 3.1.2(a), 3.1.3

Name _____ Date _____

Instructions. Answer all questions in the spaces provided. The marks for each part are shown in brackets [ ]. The total for this worksheet is **20 marks**.

1

Total: 3 marks

A car park barrier has a computer with a Von Neumann architecture. It works out how long each car has stayed.

(a) State the name of the unit in the CPU that carries out calculations. **[1]**

(b) Give **two** types of operation this unit carries out for the car park barrier. **[2]**

2

Total: 5 marks

Tick (✓) **one** box in each row to show whether each register stores an address or stores data (including instructions).

(a) Complete the table. **[5]**

Register	Address	Data
Program counter (PC)		
Memory address register (MAR)		
Memory data register (MDR)		
Current instruction register (CIR)		
Accumulator (ACC)		

3 **Total: 4 marks**

Complete the statements by writing the name of the correct register.

(a) Complete the statements. **[4]**

Statement	Register
It holds the address of the next instruction to be fetched.	
It holds the instruction that is currently being decoded and executed.	
It stores the result of a calculation carried out by the ALU.	
It holds the address of the memory location that is about to be read from or written to.	

4 **Total: 3 marks**

(a) Describe the purpose of the control unit (CU) in a CPU. **[3]**

5 **Total: 2 marks**

While the barrier's computer runs a program, the MAR holds the value 40. Later, the MDR also holds the value 40.

(a) Explain why the value 40 has a different meaning in each register. **[2]**

6 **Total: 3 marks**

The barrier's CPU has cache.

(a) Explain how cache can improve the performance of the CPU. **[3]**

Total for this worksheet: 20 marks