MODULE A SYSTEMS ARCHITECTURE · A3

Von Neumann architecture and the buses: mark scheme

~25 minutes · 20 marks · 0478 syllabus 3.1.2(a)

How to use. Award one mark per creditworthy point up to the maximum shown. **/** separates alternative words; **//** separates alternative answers for the same point. Words in (brackets) are not needed for the mark. "..." means the point builds on the one before. Credit any other valid answer that shows the same understanding.

QUESTION	ANSWER	MARKS	GUIDANCE
1(a) 0478 3.1.2(a)	Any one from: Instructions and data are stored in the same memory / RAM Programs are stored in memory (stored program concept) Instructions and data are fetched from the same memory // share the same buses	**1**	max 1
1(b) 0478 3.1.2(a)	Program counter / PC Memory address register / MAR	**2**	One mark each. First two answers only.
2(a) 0478 3.1.2(a)	Memory data register / MDR Current instruction register / CIR Program counter / PC Accumulator / ACC	**4**	One mark for each correct row, in order.
3(a) 0478 3.1.2(a)	Read or write signal: control bus Location MAR points to: address bus Instruction from RAM to MDR: data bus One direction only: address bus Value from MDR to RAM: data bus	**5**	One mark for each correct row. More than one tick in a row: no mark for that row.
4(a) 0478 3.1.2(a)	Memory address register / MAR	**1**	
4(b) 0478 3.1.2(a)	Any four from: The address (0110 1100) is placed in the MAR The address is sent (from the MAR) to RAM along the address bus The control unit sends a read signal along the control bus The price / data stored at that address is sent along the data bus ... (from RAM) to the CPU / into the MDR	**4**	max 4. Buses must be named correctly for each point.

QUESTION	ANSWER	MARKS	GUIDANCE
5(a) 0478 3.1.2(a)	Any three from: Data / instructions are read from RAM into the CPU // RAM to MDR Data is also written from the CPU to RAM // MDR to RAM ... so the data bus is bidirectional / two-way Addresses are only sent from the CPU (MAR) to RAM ... RAM never needs to send an address back to the CPU // so the address bus is unidirectional / one-way	**3**	max 3. Must give at least one reason for each bus for full marks.

Total: 20 marks