MODULE A SYSTEMS ARCHITECTURE · A4

The fetch-decode-execute (FDE) cycle: mark scheme

20 marks · Cambridge 0478 syllabus 3.1.2(b)

How to use. One mark per creditworthy point up to the maximum shown. **//** separates alternative answers. Words in (brackets) are not needed for the mark. Credit any other valid answer that shows the same understanding.

QUESTION	ANSWER	MARKS	GUIDANCE
1(a) 0478 3.1.2(b)	Current instruction register // CIR	**1**	Do not accept MDR.
1(b) 0478 3.1.2(b)	Address bus	**1**	More than one tick = 0.
2(a) 0478 3.1.2(b)	program counter // PC MAR address bus data bus MDR CIR	**6**	One mark for each correct term, in this order.
3(a) 0478 3.1.2(b)	PC: address MAR: address CIR: data / instruction ACC: data / instruction	**4**	One mark per correct row. Two ticks in a row = 0 for that row.
4(a) 0478 3.1.2(b)	151	**1**	Correct answer only.
4(b) 0478 3.1.2(b)	Any four from: The CU decodes the instruction (in the CIR) // the CU sends signals to carry it out The address 300 is placed in the MAR 300 is sent along the address bus (to RAM) A read signal is sent along the control bus The value (stored) at address 300 is sent along the data bus The value is stored in the MDR The value is copied from the MDR into the accumulator // ACC	**4**	max 4. Do not award points about fetching the instruction from address 150. Do not accept "300 is loaded into the accumulator" (300 is the address, not the value).

QUESTION	ANSWER	MARKS	GUIDANCE

5(a)
0478 3.1.2(b)
	Any three from:
	Decodes the instruction (held in the CIR) // works out what the instruction means
	Sends control signals (along the control bus) // e.g. read // write signals to memory
	Controls // coordinates the flow of data (and instructions) between the CPU components and memory
	Tells the ALU which operation to carry out
	Makes sure the stages happen in the correct order // in time with the clock
		3	max 3. Do not accept "carries out calculations" (ALU).

Total: 20 marks