MODULE A SYSTEMS ARCHITECTURE · A4

The fetch-execute cycle: mark scheme

20 marks · OCR J277 spec 1.1.1

How to use. 1 mark per bullet up to the maximum shown. **/** separates alternative answers. Words in (brackets) are not needed for the mark. Credit any other valid answer that shows the same understanding. Register-to-register transfers are not required by J277 (1.1.1 "Not required"), but credit them when they are correct.

QUESTION	ANSWER	MARKS	GUIDANCE
1(a) J277 1.1.1	To fetch and execute instructions / to run (the instructions of) programs / to process data and instructions	**1**	Allow "carries out the fetch-execute cycle". Do not accept "the brain of the computer" or "does calculations" on its own (NE).
1(b) J277 1.1.1	(Main) memory / RAM	**1**	Allow cache. Do not accept hard disk / secondary storage / ROM on its own.
2(a) J277 1.1.1	Brought from memory into the CPU: Fetch ALU adds two numbers: Execute PC incremented: Fetch Result stored in accumulator: Execute PC used to find the next address: Fetch	**5**	1 mark per correct row. 2 ticks in a row = 0 for that row.
3(a) J277 1.1.1	PC: Address MAR: Address MDR: Data Accumulator: Data	**4**	1 mark per correct row. 2 ticks in a row = 0 for that row.
4(a) J277 1.1.1	41	**1**	Correct answer only.
4(b) J277 1.1.1	Control unit / CU	**1**	Do not accept ALU / "the CPU" (NE).
4(c) J277 1.1.1	The value (stored) at address 90 is fetched / read from memory (into the CPU) (Address 90 goes into the MAR and) the value is held in the MDR The CU sends signals to the ALU / the ALU carries out the addition The ALU adds the value to the value in the accumulator The result is stored in the accumulator	**3**	1 mark per bullet, Max 3. Do not accept "the accumulator stores the calculation" for the last bullet: it stores the result. Do not award points about fetching the instruction at address 40.

QUESTION	ANSWER	MARKS	GUIDANCE
5(a) J277 1.1.1	The PC holds the address of the next instruction (to be fetched) The instruction is fetched from (main) memory / RAM (at that address) The PC is incremented / increased by 1 (to point to the next instruction) The (fetched) instruction is held in the MDR The control unit decodes the instruction / works out what it means The instruction is executed / carried out (e.g. the ALU does a calculation / data is loaded or stored) The result (of a calculation) is stored in the accumulator The cycle repeats (continuously) for the next instruction	**4**	1 mark per bullet, Max 4. Points can be in any order. Allow the PC to be incremented either before or after the instruction arrives. "Fetch, decode, execute" listed with no description = 0. Do not accept "the CPU fetches it from the hard disk".

Total: 20 marks