MODULE A SYSTEMS ARCHITECTURE · A5

CPU performance: mark scheme

~25 minutes · 20 marks · 0478 syllabus 3.1.3

How to use. Award one mark per creditworthy point up to the maximum shown. **//** separates alternative answers for the same mark. Words in (brackets) are not needed for the mark. Mark positively and credit any other valid answer.

QUESTION	ANSWER	MARKS	GUIDANCE
1(a) 0478 3.1.3	Second row ticked: the number of fetch-decode-execute cycles carried out per second	**1**	More than one tick = 0.
1(b) 0478 3.1.3	2.5 billion // 2 500 000 000 // 2500 million	**1**	
1(c) 0478 3.1.3	Any two from: More (FDE) cycles can be carried out per second So more instructions can be processed/executed per second So tasks/programs are completed in less time	**2**	max 2
2(a) 0478 3.1.3	Any two from: Small (capacity) memory Very fast (to access) // faster than RAM Inside / close to the CPU Stores frequently used data // frequently used instructions	**2**	max 2
2(b) 0478 3.1.3	Any three from: More frequently used data/instructions can be stored in cache Cache is faster to access than RAM So fewer (slower) fetches from RAM are needed // data/instructions are more likely to be found in cache So the CPU spends less time waiting (for data/instructions) So more instructions can be processed in the same time	**3**	max 3
3(a) 0478 3.1.3	Any two from: Each core can fetch, decode and execute instructions (independently) More instructions can be processed at the same time // simultaneously Tasks can be shared / split between the cores	**2**	max 2

QUESTION	ANSWER	MARKS	GUIDANCE
3(b) 0478 3.1.3	Any two from: The program (software) cannot split its task between cores // only uses one core So the extra cores are not used / are idle The clock speed (and cache size) of each core has not changed, so the one core used runs at the same speed	**2**	max 2
4(a) 0478 3.1.3	Row 1: True Row 2: False Row 3: False Row 4: True	**4**	One mark per row. Two ticks in a row = 0 for that row.
5(a) 0478 3.1.3	Cache size // increase the (size of the) cache Any two from: More frequently used data/instructions can be held in cache So fewer fetches from (slower) RAM are needed Cache is faster to access than RAM so the CPU waits less	**3**	1 mark for cache size, then max 2 for the explanation. Clock speed or cores identified = 0 for the whole part.

Total: 20 marks