

THEME A: CONCEPTS · A1.2

Data representation and computer logic — Mark scheme

34 marks · covers A1.2.1–A1.2.5

How to mark. Each creditworthy point is on its own line and ends with a semicolon (;). A line beginning with ... is an *expansion* of the line above it, so the pair is worth the marks shown. A slash (/) separates acceptable alternative wordings. Words in (brackets) are not needed for the mark. Mark positively: credit what the student has got right rather than penalising what is missing, and accept any valid alternative not listed here. Do not award more than the maximum for a part. Where a later part uses a wrong answer from an earlier part correctly, award follow-through marks (**FT**). **HL** marks parts that assess higher level only content.

Q	ANSWER	MARKS
1(a) A1.2.1	Award [1] max 182;	1
1(b) A1.2.1	Award [1] max B6; Accept 0xB6 or B6 ₁₆ .	1
1(c) A1.2.1	Award [1] max 01011101; Accept 1011101 (leading zero omitted).	1
1(d) A1.2.1	Award [2] max Award [1] for the point and [1] for the expansion. Hexadecimal is far shorter to write than binary; ...(because) one hexadecimal digit represents exactly four bits, so an 8-bit value needs only two digits instead of eight; Hexadecimal is easier for a human to read and copy accurately; ...(so) there is less chance of a transcription error than with a long string of 1s and 0s; Conversion between hexadecimal and binary is straightforward; ...(because) each hexadecimal digit maps directly onto one group of four bits (a nibble);	2
2(a) A1.2.2	Award [2] max Award [1] per point up to [2] max. Each character is given a unique number (a code point) by a character set such as ASCII or Unicode; That number is then stored as a binary pattern / a fixed number of bits; For example ASCII uses 7 or 8 bits per character, while Unicode allows many more characters to be represented; The computer stores only the binary pattern; the character is redrawn on screen from that code when displayed;	2
2(b) A1.2.2	Award [3] max Award [1] per point up to [3] max. The answer must address both quality and size.	3

Q	ANSWER	MARKS																																
	A higher sampling rate means the amplitude of the sound wave is measured more times per second; The stored samples follow the shape of the original wave more closely, so the playback is a more accurate reproduction; Higher frequencies in the recording can be captured, so the voice note sounds clearer/less muffled; More samples per second means more values must be stored, so the file size increases; The increase in size is roughly proportional to the increase in sampling rate; Beyond a certain rate the improvement is not audible, so the extra storage brings little benefit;																																	
3(a) A1.2.3	Award [1] max NAND outputs 0 only when both of its inputs are 1, and outputs 1 in every other case; Accept: the inverse/negation of AND. Accept a correct truth table.	1																																
3(b) A1.2.3 A1.2.4	Award [1] max 1; Working: (1 AND 0) = 0, (NOT 0) = 1, 0 OR 1 = 1. Award the mark for the final value only.	1																																
3(c) A1.2.3	Award [3] max Award [1] per point up to [3] max. A logic gate takes one or more binary inputs and produces a single binary output according to a fixed rule; Gates are the physical building blocks from which all digital circuits are constructed; Combining gates allows a circuit to make decisions, so a condition in a program can be carried out in hardware; Gates are used to build the arithmetic circuits inside the ALU, such as adders; Gates are used to build storage elements such as flip-flops and registers; Because everything is represented as 1s and 0s, gate operations are all a processor needs to perform any computation;	3																																
4(a) A1.2.4	Award [2] max Award [1] for the (T AND NOT R) term and [1] for OR M. V = (T AND (NOT R)) OR M; Accept any equivalent notation, for example $V = T \cdot \bar{R} + M$, or $V = (T \wedge \neg R) \vee M$. Award [1] only if one term is correct.	2																																
4(b) A1.2.4	Award [4] max Award [1] for each pair of correct rows, [4] max. Award FT from an incorrect expression in (a) if it is applied consistently. <table><tr><th>T</th><th>R</th><th>M</th><th>V</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td></tr></table>	T	R	M	V	0	0	0	0	0	0	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	0	1	1	1	1	0	0	4
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Q	ANSWER	MARKS															
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1	1	1	1														
4(c) A1.2.4	Award [1] max 1; The manual override is pressed, so the vent opens whatever the sensors read. Award FT from the candidate's own table.	1															
5(a) A1.2.5	Award [4] max Award [1] per point up to [4] max. A NOT gate (inverter) applied to input A; An AND gate with inputs A and B; A second AND gate with inputs (NOT A) and C; An OR gate taking the outputs of the two AND gates and producing Z; Standard gate symbols must be used and all inputs and the output must be labelled. Do not award the final mark if the two AND outputs are not fed into the OR gate. Accept a correct diagram drawn with the NOT shown as a bubble on the AND input.	4															
5(b) A1.2.3	Award [1] max XOR (exclusive OR);	1															
5(c) A1.2.3	Award [1] max NAND;	1															
6(a) A1.2.4	Award [2] max Award [1] for a correctly labelled map (rows A, columns BC in the order 00, 01, 11, 10) and [1] for all eight values placed correctly. <table><tr><th>Y</th><th>BC = 00</th><th>BC = 01</th><th>BC = 11</th><th>BC = 10</th></tr><tr><th>A = 0</th><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><th>A = 1</th><td>0</td><td>1</td><td>1</td><td>1</td></tr></table>	Y	BC = 00	BC = 01	BC = 11	BC = 10	A = 0	0	0	1	1	A = 1	0	1	1	1	2
Y	BC = 00	BC = 01	BC = 11	BC = 10													
A = 0	0	0	1	1													
A = 1	0	1	1	1													
6(b) A1.2.4	Award [2] max Award [1] per correct term, [2] max. Y = B OR (A AND C); The four cells where B = 1 group to give the term B; the pair where A = 1 and C = 1 groups to give the term A AND C. Accept Y = B + AC or equivalent notation. Award [1] for one correct term only. Award FT from an incorrect but correctly grouped map in (a).	2															
6(c) A1.2.4 A1.2.5	Award [2] max Award [1] for the point and [1] for the expansion. The simplified expression needs fewer gates; ... (so) the circuit costs less to manufacture / takes up less space on the chip; Fewer gates means fewer components that can fail; ... (so) the circuit is more reliable and easier to test; A signal passes through fewer gates; ... (so) propagation delay is reduced and the circuit runs faster / uses less power;	2															

Total for this paper: 34 marks