A1 COMPUTER FUNDAMENTALS · A1.1

Computer hardware and operation

The CPU, the **fetch, decode, execute** cycle, the memory hierarchy, secondary storage, compression, and cloud services. Standard level, with one HL note on **pipelining**.

01 Inside the CPU

ALU	Arithmetic and logical operations.
CU	Decodes instructions, runs the cycle.
IR	Holds the **current** instruction.
PC	Holds the address of the **next** instruction.
MAR · MDR	Address register and data register.
AC	Holds intermediate ALU results.

02 Buses

Control	CU signals. Read, write, interrupt, timing.
Data	The bits themselves. Bidirectional.
Address	CPU to memory only.

03 CPU vs GPU

CPU

Few powerful cores. Sequential and branching work. Low latency.

GPU

Thousands of simpler cores. SIMD parallel work. High throughput.

04 Fetch · Decode · Execute

01

Fetch

PC sends the next address into the MAR. The instruction is loaded into the IR via the MDR. The PC then increments.

02

Decode

The CU reads the IR, splits it into opcode and operands, and wires the correct registers into the ALU.

03

Execute

The ALU performs the operation. The result is written back to a register or to RAM. Cycle repeats.

05 Primary memory

Registers	~0.3 ns
L1 cache	~5 ns · 32–256 KB
L2 cache	~7 ns · up to 16 MB
L3 cache	~25 ns · up to 32 MB
RAM	~80 ns · gigabytes
ROM	non-volatile · BIOS

06 Secondary memory

HDD	Spinning magnetic platters. Cheap and roomy.
SSD	NAND flash, no moving parts. Faster, pricier.
eMMC	Flash on board. Budget mobile devices.
Optical	Pits and lands, read by laser.
USB / SD	Portable NAND flash.
NAS	Network-shared storage, often RAID.

07 Compression

- **Lossless**

  Reversible. Removes **redundancy**. ZIP, PNG, RLE.

- **Lossy**

  Irreversible. Discards perceptual detail. JPEG, MP3.

RLE	AAAAA becomes 5A.
Transform	DCT to the frequency domain (JPEG, MP3).

08 Cache hit and miss

Hit	The CPU finds the data near it. Very fast.
Miss	Forces a slower trip down the memory hierarchy.
Prefetch	CPU loads predicted data into cache early.
Locality	Spatial and temporal. Why prefetching works.

09 Cloud services · control rises as you move down

SaaS	Ready-to-use software in a browser. Gmail, Google Docs, Notion. You bring the data; the provider runs everything else.	LEAST CONTROL
PaaS	A hosted environment for building, deploying, and running your own apps. Database, runtime, and scaling are handled.	MID CONTROL
IaaS	Raw virtualised servers, storage, networking. AWS EC2, Azure VMs. You install the OS; you pay for what you provision.	MOST CONTROL

FINAL PASS BEFORE THE EXAM

Rapid exam tips

Eight things that lose marks in Paper 1 if you slip on them. Skim before you walk in.

01

The **PC** stores the address of the **next** instruction. The **IR** stores the **current** one. Never the same register.

02

MAR carries addresses, **MDR** carries data. The address bus and data bus follow the same split outside the CPU.

03

All cache levels are **volatile**. So is RAM. Only ROM and secondary storage survive a power-off.

04

A GPU is faster **only on parallel** tasks. CPUs still win on branching, sequential work.

05

Pipelining never speeds up a single instruction. It overlaps stages to raise **throughput**.

06

Lossless removes **redundancy**, not detail. Lossy is **irreversible**, never use it on source masters.

07

Cloud control order: **IaaS > PaaS > SaaS**. The convenience order is the reverse.

08

When describing the cycle, name **PC, MAR, MDR, IR, ALU** and where each phase reads or writes them.