

1.1 PROCESSORS, INPUT/OUTPUT AND STORAGE · 1.1.1

CPU architecture & the fetch-decode-execute cycle

Original practice questions · 39 marks · about 45 minutes · spec 1.1.1(a)(b)(e)

Instructions. Answer all questions. The number of marks is shown in brackets [] at the end of each part. Quality of written communication is assessed in the extended-response question.

1 Total: 5 marks

This question is about the components of the CPU.

- (a) State what is meant by the term *register*. [1]
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- (b) State the name of the register that holds the address of the next instruction to be fetched. [1]
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- (c) Identify the bus that carries the address of a memory location from the CPU to main memory. [1]
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- (d) State **two** different operations that can be carried out by the arithmetic logic unit (ALU). [2]
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2 Total: 7 marks

This question is about the fetch-decode-execute cycle.

- (a) Describe what happens during the **fetch** stage of the fetch-decode-execute cycle. Your answer should name the registers used. [4]
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- (b) State the name of the register that holds the instruction while it is decoded. [1]
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- (c) Explain why the program counter is incremented during the fetch stage. [2]
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-

3

Total: 8 marks

A program is being executed. The instruction currently being processed is shown below.

```
ADD 45 ; add the contents of memory address 45 to the accumulator
```

(a) Describe how the memory address register (MAR) and the memory data register (MDR) are used as the contents of address 45 are fetched during the execute stage. [4]

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(b) State the register in which the result of the addition is stored. [1]

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(c) Explain which buses are used, and the direction of travel on each, when the contents of address 45 are transferred to the CPU. [3]

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4

Total: 5 marks

This question is about registers and buses.

(a) Describe the purpose of the memory address register (MAR). [2]

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(b) Explain how the width of the address bus affects the maximum amount of memory that a computer can address. [3]

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5

Total: 5 marks

This question is about processor architecture.

(a) Describe what is meant by the **Von Neumann** architecture. [2]

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(b) State **one** way in which the Harvard architecture differs from the Von Neumann architecture. [1]

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(c) Describe **one** feature of a contemporary processor that is not part of the standard Von Neumann architecture. [2]

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