1.1 PROCESSORS, INPUT/OUTPUT AND STORAGE · 1.1.2

Types of processor — Mark scheme

36 marks · spec 1.1.2(a)(b)(c)

AO key: AO1 = knowledge & understanding · AO2 = application · AO3 = reasoned judgements. Accept any valid alternative wording; do not award the same point twice.

Q	ANSWER	AO	MARKS
1(a)	CISC = Complex Instruction Set Computer (1); RISC = Reduced Instruction Set Computer (1).	AO1	2
1(b)	Any one non-graphics use, e.g. machine learning / scientific simulation / image or video processing / financial modelling / oil exploration. (1)	AO1	1
1(c)	Carrying out more than one instruction/task at the same time (using multiple cores/ processors). (1)	AO1	1

Q	ANSWER	AO	MARKS
2(a)	Up to 4 marks across **two distinct** differences, e.g.: • CISC has a large/complex instruction set; RISC has a small/reduced one (1+1) • CISC instructions may take several cycles; RISC instructions take one cycle (1+1) • CISC programs use fewer lines of code; RISC use more (1) • CISC hardware is more complex / uses more power; RISC is simpler / uses less (1)	AO1	4
2(b)	• RISC instructions are simple and uniform / all take the same single cycle (1) • so the stages divide neatly and can be overlapped predictably (1)	AO2	2

Q	ANSWER	AO	MARKS
3	1 mark per point, max 3: • RISC uses simpler instructions / simpler hardware (1) • which consumes less power (and generates less heat) (1) • so the battery lasts longer for the same use (1)	AO2	3

Q	ANSWER	AO	MARKS
4(a)	1 mark per point, max 3: • a CPU has a few (powerful) cores (1) • a GPU has thousands of small/simpler cores (1) • a GPU is designed for parallel processing / the same operation on many data items (SIMD) (1)	AO1	3
4(b)	• an image is made of millions of pixels needing the same calculation (1) • the GPU's many cores process these in parallel / simultaneously (1) • so it is far faster than a CPU handling them sequentially (1)	AO2	3

Q	ANSWER	AO	MARKS
5(a)	• a processor containing more than one core (1) • each core can execute instructions independently / at the same time (1)	AO1	2
5(b)	Different instructions/tasks can be processed at the same time / the workload is shared across cores. (1)	AO1	1
5(c)	• the speed-up depends on the software being written to run in parallel (1) • a sequential task cannot be split, so extra cores sit idle (1)	AO2	2

Q	LEVELS-OF-RESPONSE MARK SCHEME	AO	MARKS
6	Mark using the levels descriptors below. AO1 (knowledge of CISC/RISC), AO2 (application to the smartphone) and AO3 (justified conclusion).	AO1 ×4 AO2 ×4 AO3 ×4	12

LEVEL	DESCRIPTOR
Level 3 (9–12)	Thorough discussion of several CISC/RISC differences, clearly **applied** to the smartphone (battery, heat, size, performance, pipelining), leading to a clearly **justified** conclusion. Accurate terminology; well structured.
Level 2 (5–8)	Discusses differences with **some** application to the smartphone. A conclusion is reached but justification may be partial or one-sided.
Level 1 (1–4)	Basic points about CISC and/or RISC with little application to the context and little or no justified conclusion.
0	Nothing creditworthy.

Indicative content (not exhaustive; credit any valid point):

• CISC: large complex instruction set, fewer lines of code, more complex hardware, higher power use.

• RISC: small instruction set, one-cycle instructions, more lines of code, simpler hardware, easy to pipeline, low power.

• Smartphone constraints: limited battery, heat dissipation, physical size, and the need for good performance.

• Justified conclusion: RISC (e.g. ARM) is more suitable because lower power use means longer battery life and less heat; a valid drawback (more compiler work / more RAM for code) may be credited.

Total for paper: 36 marks