1.4 DATA TYPES & STRUCTURES · 1.4.3

Logic gates & truth tables — Mark scheme

38 marks · spec 1.4.3(d)(a) · all truth tables verified

AO key: AO1 = knowledge · AO2 = application. Accept any valid notation/symbols. Truth tables verified programmatically.

Q	ANSWER	AO	MARKS
1	A and B into an AND gate, its output into a NOT gate (or a NAND gate) (1); C and D into an AND gate, and the two results into an OR gate giving Q (1). (2)	AO2	2

Q	ANSWER	AO	MARKS
2(a)	<table><tr><th>X</th><th>Y</th><th>Z</th><th>P</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></table> 1 mark per 2 correct rows (8 rows → 4 marks). (4)	AO2	4
2(b)	1. (1)	AO2	1
2(c)	NOT (inverter). (1)	AO1	1

Q	ANSWER	AO	MARKS
3(a)	`R = (A · B) + C`. (2) (1 if AND/OR correct but bracketing unclear)	AO2	2
3(b)	1 (since A·B = 1, OR C gives 1). (1)	AO2	1

Q	ANSWER	AO	MARKS
4(a)	Each pair ANDed: `(S1·S2)`, `(S1·S3)`, `(S2·S3)` (2); the three AND outputs combined with OR gate(s) to give A (2). (Accept any circuit equal to A = S1·S2 + S1·S3 + S2·S3.) (4)	AO2	4
4(b)	<table><tr><th>S1</th><th>S2</th><th>S3</th><th>A</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></table> 1 mark per 2 correct rows. A = 1 exactly when two or three sensors are 1. (4)	AO2	4

Q	ANSWER	AO	MARKS
5(a)	<table><tr><th>GATE</th><th>AND</th><th>OR</th><th>XOR</th><th>NAND</th></tr><tr><td>OUTPUT</td><td>0</td><td>1</td><td>1</td><td>1</td></tr></table> 1 mark each (A = 1, B = 0). (4)	AO2	4
5(b)	NAND. (1)	AO1	1
5(c)	XOR. (1)	AO1	1

Q	ANSWER	AO	MARKS
6(a)	<table><tr><th>A</th><th>B</th><th>C</th><th>M</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></table> 1 mark per 2 correct rows. (4)	AO2	4
6(b)	When A = 0, M outputs the value of C (1); when A = 1, M outputs the value of B (1) (A selects between inputs B and C). (2)	AO2	2

Q	ANSWER	AO	MARKS
7(a)	XOR. (1)	AO1	1
7(b)	`(A · ¬B) + (¬A · B)`. (2)	AO2	2
7(c)	¬A and ¬B from NOT gates (1); `A·¬B` from an AND gate (1); `¬A·B` from an AND gate (1); the two AND outputs into an OR gate giving the output (1). (4)	AO2	4

Total for worksheet: 38 marks